CLAIMS

What is claimed is:

1. A processing element comprising:

an instruction buffer;

a first most often (MO) buffer coupled to the instruction buffer; and

an execution unit coupled to the instruction buffer and the first MO buffer, wherein the execution unit is adaptable to execute instructions stored within the first MO buffer based upon a first predetermined profile.

2. The processing element of claim 1 further comprising a second MO buffer coupled to the instruction buffer and the execution unit, wherein the execution unit is adaptable to execute instructions stored within the second MO buffer based upon a second predetermined profile.

3. The processing element of claim 2 further comprising a decode module coupled to the second most often (MO) buffer coupled to the instruction buffer, the first MO buffer, the second MO buffer and the execution unit.

4. The processing element of claim 3 wherein the decode module determines whether an instruction is to be stored in the first MO buffer or the second MO buffer upon decoding the instruction.

5. The processing element of claim 4 further comprising:

a first profile buffer coupled to the first MO buffer, wherein the first profile buffer stores the first predetermined profile; and

a second profile buffer coupled to the second MO buffer, wherein the second profile buffer stores the second predetermined profile.

6. The processing element of claim 5 wherein the first and second predetermined

profiles each include a plurality of profile bits, each profile bit indicating whether a corresponding instruction is to be executed at the execution unit during a particular instruction fetch cycle.

7. The processing element of claim 6 further comprising:

a first profile pointer coupled to the first profile buffer; and

a second profile pointer coupled to the second profile buffer.

8. The processing element of claim 7 wherein the first profile pointer points to a first profile bit of the first predetermined profile during a first instruction fetch cycle.

9. The processing element of claim 8 wherein an instruction stored in the first MO buffer is executed at the execution unit during the first instruction fetch cycle if the first profile bit is active.

10. The processing element of claim 8 wherein an instruction stored in the instruction buffer is executed at the execution unit during the first instruction fetch cycle if the first profile bit is inactive.

11. A digital signal processor (DSP) comprising:

a plurality of processing elements, wherein each of the processing elements comprises:

an instruction buffer;

a first most often (MO) buffer coupled to the instruction buffer; and

an execution unit coupled to the instruction buffer and the first MO buffer, wherein the execution unit is adaptable to execute instructions stored within the first MO buffer based upon a first predetermined profile.

12. The DSP of claim 11 wherein each processing element further comprises a second MO buffer coupled to the instruction buffer and the execution unit, wherein the execution

unit is adaptable to execute instructions stored within the second MO buffer based upon a second predetermined profile.

13. The DSP of claim 12 wherein each processing element further comprises a decode module coupled to the second most often (MO) buffer coupled to the instruction buffer, the first MO buffer, the second MO buffer and the execution unit.

14. The DSP of claim 13 wherein the decode module determines whether an instruction is to be stored in the first MO buffer or the second MO buffer upon decoding the instruction.

15. The DSP of claim 14 wherein each processing element further comprises:

a first profile buffer coupled to the first MO buffer, wherein the first profile buffer stores the first predetermined profile; and

a second profile buffer coupled to the second MO buffer, wherein the second profile buffer stores the second predetermined profile.

16. The DSP of claim 5 wherein the first and second predetermined profiles each include a plurality of profile bits, each profile bit indicating whether a corresponding instruction is to be executed at the execution unit during a particular instruction fetch cycle.

17. The DSP of claim 16 wherein each processing element further comprises:

a first profile pointer coupled to the first profile buffer; and

a second profile pointer coupled to the second profile buffer.

18. The DSP of claim 17 wherein the first profile pointer points to a first profile bit of the first predetermined profile during a first instruction fetch cycle.

19. A method comprising:

receiving a first instruction at an instruction buffer;

determining whether the first instruction has been designated to be retrieved from a first buffer in order to be executed; and

if so, retrieving the first instruction from the first buffer;

otherwise, retrieving the buffer from a second buffer.

20. The method of claim 19 further comprising executing the first instruction after it has been retrieved from the first buffer.

21. The method of claim 19 further comprising:

determining whether the first instruction has been designated to be stored in the first buffer if the first instruction has not been designated to be retrieved from the first buffer in order to be executed;

if so, storing the first instruction in the first buffer; and

executing the first instruction after it has been retrieved from the second buffer.

22. The method of claim 21 further comprising:

determining whether the first instruction includes a command to load a profile if the first instruction has not been designated to be stored in the first buffer;

if so, loading the profile in a third buffer; and

executing the first instruction after it has been retrieved from the first buffer.

23. The method of claim 22 further comprising executing the first instruction after it has been retrieved from the second buffer if it is determined that the first instruction does not include a command to a load a profile if the first instruction has not been designated to be stored in the first buffer.

24. An article of manufacture including one or more computer readable media that embody a program of instructions, wherein the program of instructions, when executed

by a processing unit, causes the processing unit to:

receive a first instruction at an instruction buffer;

determine whether the first instruction has been designated to be retrieved from a first buffer in order to be executed; and

if so, retrieve the first instruction from the first buffer;

otherwise, retrieve the first instruction from a second buffer.

25. The method of claim 24 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to execute the first instruction after it has been retrieved from the first buffer.

26. The method of claim 24 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to:

determine whether the first instruction has been designated to be stored in the first buffer if the first instruction has not been designated to be retrieved from the first buffer in order to be executed;

if so, store the first instruction in the first buffer; and

execute the first instruction after it has been retrieved from the second buffer.

27. The method of claim 26 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to:

determine whether the first instruction includes a command to a load a profile if the first instruction has not been designated to be stored in the first buffer;

if so, load the profile in a third buffer; and

execute the first instruction after it has been retrieved from the first buffer.

28. The method of claim 27 wherein the program of instructions, when executed by a processing unit, further causes the processing unit to execute the first instruction after it has been retrieved from the second buffer if it is determined that the first instruction does

not include a command to a load a profile if the first instruction has not been designated to be stored in the first buffer.